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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,291	10/02/2000	Behnam Tabrizi	1920/107	4310

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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,291	TABRIZI, BEHNAM	
	Examin r	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-32 and 34-39* is/are pending in the application.

4a) Of the above claim(s) *23-31 and 37-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-22,32 and 34-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *08 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's amendment field on October 8, 2002 has been received and entered in the case.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following limitation in claims 1, 14, 16, 21 and 32 "a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 13, line 2, "the silicon package" lacks antecedent basis.

In claim 18, line 4, "the bottom terminal" lacks antecedent basis.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 2, 5 ~ 22, 32 and 34 ~ 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Thomas.

Regarding claim 1, Thomas discloses in Fig. 4b and column 3, lines 47 ~ 59 an electronic component comprising:

- an electronic device package (10) including a silicon wafer (22, 24, 26 and 28) having a recess (30), the recess including a conductive region (14a); and

- a bare die electronic device (18) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess, and wherein the non-top terminal is electrically coupled to the conductive region.

Regarding claim 2, Thomas discloses in Fig. 4b the conductive region (14a) being formed by metallization.

Regarding claim 5, Thomas discloses in Fig. 4b the device (18) being physically coupled to the package by the conductive region.

Regarding claim 6, Thomas discloses in column 8, lines 1 ~ 2 a dielectric that is deposited so as to at least partially fill the recess.

Regarding claim 7, Thomas discloses in column 6, lines 39 ~ 45 a plurality of metallized bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

Regarding claim 8, Thomas discloses in Fig. 4b and column 6, lines 39 ~ 45 the package (10) including a top and a bottom; and the bumps are located above the top of the package.

Regarding claim 9, Thomas discloses in Fig. 4b the device (18) being a vertical device and the bottom of the device is coupled to the package in the recess.

Regarding claim 10, Thomas discloses in Fig. 4b a second conductive region (16) coupled to a terminal other than the non-top terminal.

Regarding claim 11, Thomas discloses in Fig. 4b a plurality of contact including at least a first contact (12b) and a second contact (12a), the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal.

Regarding claim 12, Thomas discloses in column 7, lines 56 ~ 67 the plurality of contacts reside in the same plane.

Regarding claim 13, Thomas discloses in Fig. 4b a second layer of dielectric (34) completely covering the silicon package and the device except for the plurality of contacts.

Regarding claim 14, Thomas discloses in Fig. 4b and column 3, lines 47 ~ 59 an electronic component comprising:

- an electronic component package (10) including a silicon wafer (22, 24, 26 and 28) having a recess (30), the recess including a first conductive region (14a); and
- a bare die electronic device (18) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in the recess, wherein the non-top terminal is electrically coupled to the first conductive region (14a) and the top terminal is electrically coupled to a second conductive region (16a), and wherein at least a portion of the first and second conductive regions are essentially planar.

Regarding claim 15, Thomas discloses in Fig. 4b the second conductive region (16a) being a solder bump.

Regarding claim 16, Thomas discloses in Fig. 4b and column 3, lines 47 ~ 59 an electronic component comprising:

- an electronic component package (10) including a silicon wafer (22, 24, 26 and 28) having a recess (30), the recess including a first conductive region (14a); and
- an electronic device (12) having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the

device being disposed in the recess, wherein the non-top terminal is electrically coupled to the conductive region.

Regarding claim 17, Thomas discloses in Fig. 4b and column 7, lines 56 ~ 67 one of the terminals of the device (18) being a top contact located at the top of the device; and the package (10) having a package top, wherein the package top also including a contact (12b) coupled electrically via the conductive region to the non-top terminal.

Regarding claim 18, Thomas discloses in Fig. 4b the conductive region (14a) comprising a layer of metal; and the electronic device (18) resides within the recess and the metal is electrically coupled to the bottom terminal of the device.

Regarding claim 19, Thomas discloses in Fig. 4b and column 8, lines 1 ~ 2 a layer of insulation coupling the silicon package to the electronic device.

Regarding claim 20, Thomas discloses in Fig. 4b and column 7, lines 56 ~ 67 the metal of the conductive region (14a) extending to a portion of the package top, the electronic component further comprising: a bottom contact electrically coupled to the metal on the package top.

Regarding claim 21, Thomas discloses in Fig. 4b, column 3, lines 47 ~ 59 and column 8, lines 1 ~ 2 an electronic component comprising:

- an electronic device (18) having a first terminal and a second terminal, wherein a first dimension is defined therebetween;
- an electronic device package (10) having a first surface, the package including a silicon wafer having a recess (opening in layer 24) on the first surface that has a depth that is substantially equal to the first dimension, the package further having a layer of metal (14a) applied to the recess and to a portion of the first surface, wherein the

electronic device resides within the recess and the second terminal is coupled to the layer of metal; and

- a layer of insulation coupling the electronic device to the silicon wafer.

Regarding claim 22, Thomas discloses in Fig. 4b and column 7, lines 56 ~ 67 a first contact coupled to the first terminal; and a second contact coupled to the metal residing on the first surface of the package.

Regarding claim 32, Thomas discloses in Fig. 4b, column 3, lines 47 ~ 59 and column 8, lines 1 ~ 2 an electronic component comprising:

- a non-molded electronic component package (10) having a package top and a silicon wafer including a recess (30);
- a planar bare die electronic device (18) having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess; and
- a planarizing material filling the recess not occupied by the device to substantially create a level plane that includes the top of the device.

Regarding claim 34, Thomas discloses in Fig. 4b a metallization layer (14a).

Regarding claim 35, Thomas discloses in Fig. 4b and column 7, lines 56 ~ 67 the metallization layer couples each contact to a redistribution point on the package top, and each contact remains electrically distinct.

Regarding claim 36, Thomas discloses in Fig. 4b and column 6, lines 39 ~ 45 a plurality of conductive bumps (14), each bump being disposed at a redistribution point.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas in view of Yoshida et al. or Oji et al.

Thomas discloses the claimed invention except the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. However, Yoshida et al. or Oji et al. discloses the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Thomas by adding the conductive region as taught by Yoshida et al. or Oji et al. The ordinary artisan would have been motivated to modify Thomas in the manner described above for at least the purpose of increasing adhesive strength between the conductive region and the device.

Response to Arguments

10. Applicant's arguments with respect to claims 1, 9, 14, 16, 21, 22 and 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Angiulli et al. discloses in column 2, lines 16 ~ 19 a packaging wiring substrate can be a silicon wafer. Koike discloses a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
November 19, 2002

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800